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Description

INTEGRATED REDUCED MEDIA INDEPENDENT INTERFACE

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to an integrated reduced media independent interface, and more specifically, to an integrated reduced media independent interface for reducing pin count and related method.

[0003] 2. Description of the Prior Art

[0004] In modern society, information flows acrossnetworks so that people can share information and technology. With the growing need for bandwidth, significant development is occurring in the area of high-speed networking. In the future, Ethernet will not only be used in local area networks (LANs) but also in wide area networks (WANs).

[0005] In the related specifications of Ethernet, the media independent interface for connecting a medium access control

circuit (MAC circuit) and a physical circuit (PHY Circuit) is replaced by the reduced media independent interface (RMII). The specification of the reduced media independent interface (RMII) is the same as the specification of the media independent interface (MII), and these specifications are essentially according to IEEE 802.3 and IEEE 802.3u.

[0006] Comparing the reduced media independent interface (RMII) with the media independent interface according to the prior art, the most important improvement is that chip pin count is reduced. In the manufacture of chips and in packaging techniques, ping count influences cost. The greater the number of pins is, the higher the cost is. This means that the reduced media independent interface provides a good choice of interface count with the IEEE 802.3u specification. Please refer to Fig.1. Fig.1 is a schematic diagram of the reduced media independent interface (RMII). From the above, the reduced media independent interface (RMII) 10 is used for connecting a medium access control circuit (MAC circuit) 12 and a physical circuit 14 (PHY circuit). The reduced media independent interface can be separated into two parts by the transmission direction of signals and data: a transmitter

16 and a receiver 18. In the transmitter 16 the transmission direction of signals is from the medium access control circuit (MAC circuit) 12 to the physical circuit 14. In the receiver 18, the transmission direction of signals and data is from the physical circuit 18 to the medium access control circuit (MAC circuit) 12. The reduced media independent interface can be separated into a plurality of specialized interfaces. The interfaces in the transmitter 16 include a transmission data interface (TXD) and a transmission-enabling interface (TX_EN). The transmission data interface is used for transmitting data from the medium access control circuit (MAC circuit) 12 to the physical circuit (PHY circuit). In general, there are two transmission speeds: 10Mb/s and 100Nb/s. When the transmission-enabling interface (TX_EN) outputs a high voltage in an assert mode, the physical circuit 14 receives the data transmitted from the medium access control circuit (MAC circuit) 12 through the transmission data interface. In other words, when the transmission-enabling interface (TX_EN) is not in assert mode (ex: the transmission-enabling interface outputs a predetermined low-voltage signal), the physical circuit does not receive data from the medium access control circuit (MAC circuit) 12.

[0007] Please refer to Fig.1. The receiver 18 of the reduced media independent interface (RMII) 10 includes a reference clock interface (REF_CLK), a receiving-enabling interface, an error-detecting interface (RX_ER) and a data receiving interface (RXD). The reference clock interface is used for providing a reference clock to the specialized interfaces of the reduced media independent interface 10 (RMII) that include the transmission data interface (TXD), the transmission-enabling interface (TX_EN), the receiving-enabling interface (CRS_DV), the error-detecting interface (RX_ER), and the data receiving interface (RXD). The reference clock is generated by the MAC circuit 12 or by an external source. Therefore, the detail interfaces of the reduced media independent interface 10 (RMII) operate synchronously according to the reference clock. Please refer to the Fig.2. Fig.2 is a time sequence diagram relating to the plurality of interfaces of the receiver 18 in the reduced media independent interface 10 (RMII). The data receiving interface (RXD) is used for transmitting data from the physical circuit 14 (PHY circuit) to the medium access control circuit (MAC circuit) 12. When the reduced media independent interface 10 (RMII) is in an idle mode (the receiving-enabling interface is at a predetermined low volt-

age), the medium access control circuit (MAC circuit) 12 rejects data from the physical circuit (PHY circuit) 14 through the data receiving interface. When the receiver 18 operates, the physical circuit (PHY circuit) 14 does not detect an invalid code or other error information and the physical circuit 14 (PHY circuit) does not detect data to be transmitted, the reduced media independent interface 10 (RMII) is not in the idle mode, the receiving-enabling interface is set to a predetermined high voltage, the error-detecting interface (RX_ER) is at a low voltage, the reduced media independent interface 10 (RMII) is in a transmission-enabling mode, and the medium access control circuit (MAC circuit) 12 receives data from the physical circuit 14 through the data receiving interface (RXD). When the physical circuit (PHY circuit) detects the invalid code or other error information, the error-detecting interface is in a predetermined high voltage and the medium access control circuit (MAC circuit) 12 detects data from the physical circuit 14 (PHY circuit) as invalid data. At this moment, the reduced media independent interface is in an error-detection mode, and the medium access control circuit (MAC circuit) 12 rejects data from the data receiving interface 14. So, the error-detecting interface (RX_ER) can

improve the rate of transmission of correct data in the reduced media independent interface 10 (RMII).

[0008] However, in the requirement for reducing spin count and in consideration of conforming the specification of the reduced media independent interface 10 (RMII), when the prior art reduced media independent interface is designed adaptively, it is better to further reduce the pin count of the reduced media independent interface lower the cost of the related products.

SUMMARY OF INVENTION

[0009] It is therefore a primary objective of the claimed invention to provide an integrated reduced independent interface.

[0010] According to the claimed inventionan integrated reduced media independent interface (Integrated RMII) for interconnecting a medium access control circuit (MAC circuit) and a physical circuit (PHY Circuit) includes a transmission data interface (TXD) for transmitting data from a media control circuit to the physical circuit (PHY circuit), a transmission-enabling interface (TX_EN) for controlling the transmission data interface (TXD), a reference clock (REF_CLK) interface for providing a reference clock to the integrated reduced media independent interface (Integrated RMII), a receiving-enabling interface (CRS_DV)

for detecting a low-voltage indicating an error-detection mode and an idle mode, and a high voltage indicating a transmission-enabling mode and a data receiving interface (RXD) for transmitting the data from the physical circuit (PHY circuit) to the medium access control circuit (MAC circuit). Certainly, the integrated RMII could further comprise some parts being nothing about the transmittion of the data. However, the parts are independent on the character(s) of the invention, and would not be discussed in the specification.

[0011] According to the claimed invention a method for transmitting data with an integrated reduced media independent interface (Integrated RMII) comprises the following steps: using the physical circuit (PHY circuit) to provide a low voltage to the receiving-enabling interface in a error-detection mode or an idle mode; using the physical circuit (PHY circuit) to provide a high voltage to the receiving-enabling interface in a transmission-enabling mode; using the medium access control circuit (MAC circuit) to receive the data transmitted from the physical circuit (PHY circuit) via the data receiving interface when the receiving-enabling interface outputs a high voltage; using the medium access control circuit (MAC circuit) to reject the data

transmitted from the physical circuit (PHY circuit) via the data receiving interface when the receiving-enabling interface outputs a low voltage.

[0012] Significantly, to compare with the prior art, the invention integrates the error-detecting interface into the receiving-enabling interface so that the two functions of two conventional interface is performed by the presented integrated RMII interface. Therefore, the number of pins is reduced and then both the required material and the fabrication cost are reduced, but the functions of the presented integrated RMII interface are not degraded.

Brief Description of Drawings

[0013] Fig.1 is a schematic diagram of the reduced media independent interface (RMII) according to the prior art.

[0014] Fig.2 is a time sequence diagram of operation of a plurality of interfaces in the reduced media independent interface (RMII) of Fig.1.

[0015] Fig.3 is a schematic diagram of the integrated reduced media independent interface (RMII) according to the present invention.

[0016] Fig.4 is a time sequence diagram of operation of a plurality of interfaces in the integrated reduced media independent interface (RMII) of Fig.3.

DETAILED DESCRIPTION

[0017] The technical features of the invention are essentially based on the specification of reduced media independent interface according to IEEE 802.3 and 802.3u. The error-detecting interface, especially the function(s) of the error-detecting interface, is combined in the receiving-enabling interface in the invention without the external error-detecting interface (RX_ER). Please refer to Fig.3. Fig.3 is a schematic diagram of the integrated reduced media independent interface (RMII). Compared to the prior art, the integrated reduce media independent interface 20 is also used for connecting a medium access control circuit (MAC circuit) and a physical circuit 24 (PHY circuit). However, the integrated reduced media independent interface 20 without the external error-detecting interface (RX_ER) comprises a transmission data interface (TXD) for transmitting data from the medium access control circuit (MAC circuit) 22 to the physical circuit 24 (PHY circuit), a transmission-enabling interface (TX_EN) for controlling the transmission data interface (TXD), a reference clock interface for providing a reference clock, a receiving-enabling interface (CRS_DV) and a data receiving interface (RXD) for transmitting data from the physical circuit 24 (PHY circuit)

to the MAC circuit 22. The reference clock is generated by a medium access control circuit (MAC circuit) 22 or an external source. The transmission interface (TXD), the transmission-enabling interface (TX_EN), the receiving-enabling interface (CRS_DV) and the data receiving interface (RXD) operate synchronously according to the reference clock.

[0018] Please refer to Fig.4. Fig.4 is a time sequence diagram of operation of a plurality of interfaces in the integrated reduced media independent interface (RMII) 20 of Fig.3. In the embodiment, the data receiving interface (RXD) is a binary transmission cable separated into two lines RXD[0] and RXD[1]. The data receiving interface RXD(RXD[0], RXD[1]) could transmits a binary data from the physical circuit 24 (PHY circuit) to the medium access control circuit (MAC circuit) 22 in a clock period of the reference clock. When the receiving-enabling interface is in the idle mode (the receiving-enabling interface is at a predetermined low voltage), the medium access control circuit (MAC circuit) 22 does not receive data transmitted from the physical circuit (PHY circuit) 24 through the data receiving interface (RXD). When the physical circuit (PHY circuit) 24 does not detect any invalid code or other error in-

formation and the physical circuit (PHY circuit) 24 detects data to be transmitted, the integrated reduced independent interface 20 is not in the idle mode. When the receiving-enabling interface is at a predetermined high voltage, the integrated reduced independent interface 20 is in a transmission-enabling mode. The medium access control circuit (MAC circuit) 22 receives data from the physical circuit (PHY circuit) 24 through the data receiving interface (RXD). When the physical circuit (PHY circuit) 24 detects the invalid code or other error information, the receiving-enabling interface (CRS_DV) is used for detecting the error as the structure of the integrated reduce media independent interface 20 is without the error-detecting interface. The receiving-enabling interface (CRS_DV) is set to a predetermined low voltage, and the MAC circuit 22 detects data transmitted from the data receiving interface (RXD) as invalid data and does not receive this data. At this moment, the integrated reduced media independent interface 20 is in an error-detection mode. In addition, the data receiving interface replaces the error-detecting interface of Fig.1.

[0019] Comparing Fig.2 with the time sequence diagram in Fig.4, the features of the invention are illustrated. In Fig.2, the

error-detecting interface (RX_ER) achieves the related function by raising the voltage in the error-detection mode. At the same time sample point, as shown in Fig.4 the receiving-enabling interface (CRS_DV) lowers the voltage to achieve the related function in the integrated reduced media independent interface 20 of the invention to make the medium access control circuit (MAC circuit) 22 detect the transmitted data as invalid data and not receive such data.

[0020] In conclusion, under the controlling of the physical circuit 24 (PHY circuit) of Fig.3, the error-detecting interface (RX_ER) is combined into the receiving-enabling interface (CRS_DV) and the receiving-enabling interface (CRS_DV) is at a low voltage in the error-detection mode (when the physical circuit (PHY circuit) detects an invalid code or other error information), and in an original idle mode (during system reset, when there is no transmission data, or when the physical circuit 24 (or the medium access control circuit (MAC circuit) 22 is not operating.). The receiving-enabling interface (CRS_DV) is at a high voltage in a transmission-enabling mode (when the physical circuit 24 does not detect an invalid code or other error information and detects that data is to be transmitted). This is

because the data receiving interface (RXD) outputting a high voltage is specified in the specification of the reduced media independent interface (RMII) according to IEEE 802.3 and IEEE 802.3u. The medium access control circuit (MAC circuit) 22 receives data from the physical circuit 24 (PHY circuit) through the data receiving interface (RXD). When the receiving-enabling interface (CRS_DV) outputs a low voltage, the medium access control circuit (MAC circuit) 22 rejects data from the physical circuit 24 (PHY circuit) through the data receiving interface (RXD). Thus, it is not necessary to use the increases of the voltage in the error-detecting interface to alert the system. In the invention, a voltage drop in the receiving-enabling interface is used to achieve the goal of alerting to and rejecting receiving data. In this way, compared to the prior art, the pin count of the reduced media independent interface 24 (RMII) of Fig.3 according to the invention is reduced to less than the pin count of the reduced media independent interface 10 (RMII) of Fig.1. In addition, the Ethernet system resources of the integrated reduced media independent interface 20 according to the invention can be simplified.

[0021] Those skilled in the art will readily observe that numerous

modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be constructed as limited only by the metes and bounds of the appended claims.